

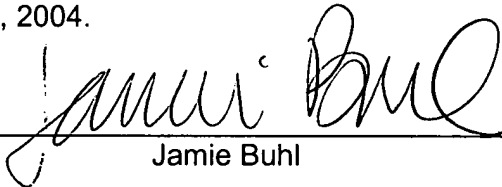


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: Sunil Kumar Sharma
Title of Invention: **MAPPING OF PROGRAMMABLE LOGIC DEVICES**
Serial No.: 10/675,908
Filing Date: September 29, 2003
Attorney Dkt. No.: 11556(P-54)USA; 2110-80-3

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Jamie Buhl

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR § 1.97

March 4, 2004

TO THE COMMISSIONER FOR PATENTS:

In compliance with the duty of disclosure under 37 CFR § 1.56, Applicant submits herewith patents, publications, or other information for consideration during the examination of this application.

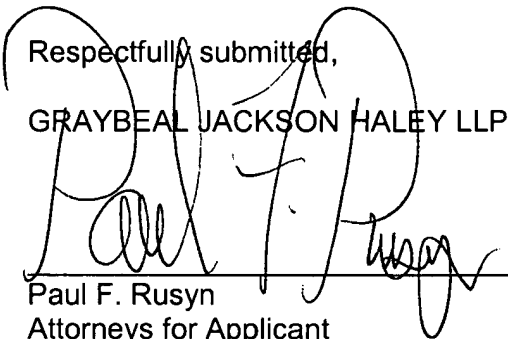
In accordance with 37 CFR § 1.97, the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made nor that the information cited in the statement is or is considered to be "material" to patentability as defined in 37 CFR § 1.56(b).

X Charge any additional fees to Deposit Account No. 07-1897

X A postcard as acknowledgement of receipt of Form PTO-1449 and copies of the documents cited in the attached form are enclosed.

Respectfully submitted,

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Form PTO-1449 U.S. Department of Commerce (Rev 7-80) PATENT AND TRADEMARK OFFICE		Attorney Docket No.: 11556(P-54)USA; 2110-80-3		SERIAL NO. 10/675,908			
LIST OF PRIOR ART CITED BY APPLICANT (Use Several Sheets if necessary) <input type="checkbox"/>		APPLICANT: <u>Sunil Kumar Sharma</u>		FILING DATE: <u>September 29, 2003</u> GROUP: <u>2676</u>			
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		Kuang-Chien Chen, Jason Cong, Yuzheng Ding, Andrew Kahng, Peter Trajmar; <i>DAG-Map: Graph Based FPGA Technology Mapping For Delay Optimization</i> ; IEEE Design and test of computers, pp 7-20, sept.1992.					
		Jason Cong and Yuzheng Ding; <i>An Optimal Technology Mapping Algorithm for Delay Optimization in Lookup -Table Based FPGA Designs</i> ; IEEE Trans. On Computer Aided Design of Integrated Circuits and Systems CAD, Vol.13, pp 1-12 Jan 1994.					
		Jason Cong and Yuzheng Ding; <i>On Area/Depth Trade-off in LUT-Based FPGA Technology Mapping</i> ; 30 th ACM/IEEE design Automation Conference (DAC), pp. 213-218, 1993.					
		Jason Cong and Yuzheng Ding; <i>Beyond the Combinatorial Limit in Depth Minimization for LUT-Based FPGA Designs</i> ; IEEE/ACM International Conference on Computer Aided Design (ICCAD), pp. 110-114, Nov. 1993.					
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw Line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							